			Revisions		217230		В
ŀ	AL	Rev	Doscription	Chk	Date	Approved	
		Α	ENGRG RELEASE •	BN	11-8-78	·	
î î		В	ADDED NOTE 2: CUT ETCH TO J12 FINGERS (COMP. SIDE)	BN	2/28/79		
١.	×	С	REVISED NOTE 2. ADD ITEM 2,10,11 TO M/L.	BN	4/24/79		

## ENGAGE PRELEASE

Do Not Scale Drawing

1 OF 4

Dist Code SPG NTMB1-PWASSY.SIL (PNTMB-PWASSY.DM) Notes Unless Specified Drawn **Xerox Corporation** These drawings and specifications **NISHIMURA** XEROX: and the data contained therein, El Segundo, California are the exclusive property of 1. Tolerances BN 2/28/79 Xerox Corporation and/or Rank Angular Xerox, Ltd. Issued in strict confi-£0. ★ xx. dence and shall not, without the .xxx. + .010 +1/20 Appr. ASSEMBLY, PRINTED WIRINGprior written permission of Xerox Corporation or Rank Xorox, Ltd. be 2. Break All Sharp Edges Material .010 Approx reproduced,copied or used for \* MOTHERBOARD \/ any purpose whatsoever except 3. Mach. Surfaces manufacture of articles for (NOTETAKER) ox Corporation or Rank Xerox. 4.All Dim. in inches Chango Letter Dwg. No. Finish Code Ident Model No. Hrst Uso NOTETAKER 18338 Α 217230 3 C Next Assy.

Scale NONE

217684

First Uso

## NOTES: UNLESS OTHERWISE SPECIFIED

- 1. ASSEMBLE PER MODULE ASSEMBLY SPEC, DWG NO. 216207.
- 2. THE FOLLOWING MODIFICATIONS ARE REQUIRED USING "A" REVISION PRINTED WIRING BOARDS:
  - 1) ADD RESISTOR, R3 (ITEM 11) BETWEEN J12-14 TO J12-17 (ETCH SIDE).
  - 2) CUT ETCH TO J9 PIN 19 (ETCH SIDE).
  - 3) CUT BOTH ETCH TO J9 PIN 22 (ETCH SIDE).
  - 4) CUT BOTH ETCH TO J9 PIN 72 (ETCH SIDE).
  - 5) CUT ETCH BETWEEN J9 PIN 71 TO J8 PIN 21 (ETCH SIDE).
  - 6) ADD JUMPER FROM J12 PIN 9 TO J8 PIN 22 (ETCH SIDE).
  - 7) ADD JUMPER FROM J12 PIN 10 TO J8 PIN 72 (ETCH SIDE).
  - 8) REMOVE CONNECTOR J9 FROM BOARD AND CUT GROUND PLANE AROUND J9 PIN 20 AND J9 PIN 70 (ISOLATE BOTH PINS FROM GROUND).
    REINSTALL J9 CONNECTOR ON BOARD.

NTMB2-PWASSY.SIL

se drawings and specifications, and the data calned therein, are the exclusive property of Xerox Corporation and or Rank Xerox, Ltd. Issued in strict confidence and shall not, without the prior written permission of Xerox Corporation Rank Xerox, Ltd., be reproduced, copied or used for any purpose whatsoever, except the manufacture of articles for Xerox Corporation or Rank Xerox, Ltd.

ASSEMBLY, PW-

Title

Xerox Corporation
El Segundo, California

XEROX

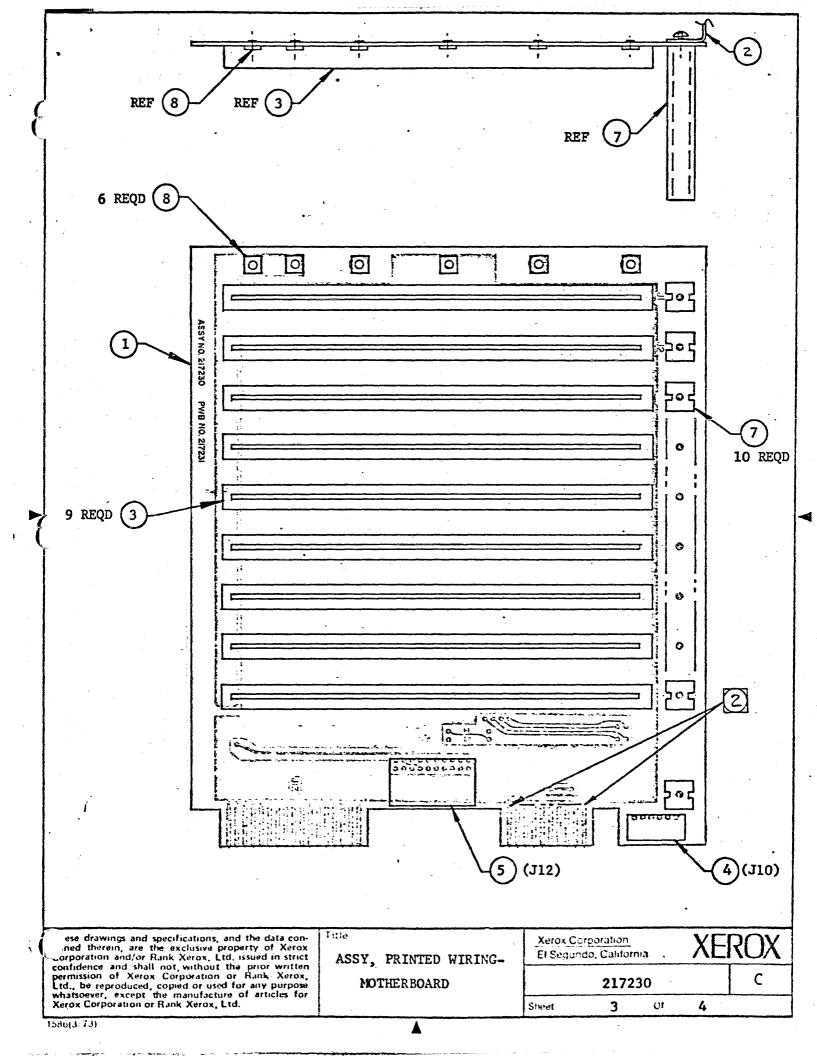
4

217230

C

Sheet 2

10



## View from etch side

<b>(</b> "he	e 6 pins connector		J9		1 10		17		J6		
1		_	+		J8		J7		-t		<b> </b>
2 3	TABXO TABYO	1_	+ 12v	+ 12v	+ 12v	+ 12v	51				
4	TABX1	2_	+ 12v	+ 12v	+ 12v	+ 12v	+ 12 v	+ 12v	+ 12v	+ 12v	52
5 6	TABY1	3_ 4	PageMode'	****	PageMode*	****	PageMode'	****	PageMode'	****	53
U			GoMem'	VSYNC'	GoMem*	VSYNC'	GoMem'	VSYNC'	GoMem'	VSYNC'	54
		5_	-20V	-20V	-20V	-20 <b>V</b>	-20V	-20V	-20V	-20V	55
Display Interface			BusLock'	Videα	BusLock'	Videα	BusLock'	Videa	BusLock'	Videox	56
10			BusClkDly'	HSync	BusClkDly'	HSync	BusClkDly'	HSync	BusClkDly'	HSync	57
9 8	Vert Drive (VSYNC') Video Input	8_ 9	ProcBoot'	ParErr	ProcBoot'	ParErr	ProcBoot'	ParFrr	ProcBoot'	ParErr	58
7	12V DC Input		ProcInt'	DataReady	Procint'	DataReady	Procint'	DataReady	Procint'	DataReady	59
6 5	Horiz Drive (HSync) Arc Ground			Gnd Bus Bog 4	Gnd BucBogO'	Gnd Bus Bog 4	Gnd Rus RogO'	Gnd BusReq4'	Gnd Bus BogO	Gnd Ruc Road*	60
4		11_	BusReq0'	BusReq4'	BusReq0'	BusReq4'	BusReq0'		BusReq0'	BusReq4'	61
3 2		12	BusReq1'	BusReq5'	BusReq1'	BusReq5'	BusReq1'	BusReq5'	BusReq1'	BusReq5'	62
1	Horizontal Grd	13_ 14	BusReq2' BusReq3'	BusReq6' BusReq7'	BusReq2' BusReq3'	BusReq6' BusReq7'	BusReq2' BusReq3'	BusReq6' BusReq7'	BusReq2' BusReq3'	BusReq6' BusReq7'	63
			Bootsw +	TABX0	Bootsw +	TABXO	Bootsw +	TABX0	Bootsw +	TABXO	64 65
			Bootsw-	TABYO	Bootsw-	TABYO	Bootsw-	TABYO	Bootsw-	TABYO	66
			CharCtr	TABX1	CharCtr	TABX1	CharCtr	TABYO	CharCtr	TABX1	67
				TABY1	CharPwr	TABY1	CharPwr	TABY1	CharPwr	TABY1	68
-		<del>10≥</del> 19	96Khz	***	96Khz	***	96Khz	***	96Khz	***	69
The	20 pins Connector	20	Gnd	Gnd	Gnd	Gnd	Gnd	Gnd	Gnd	Gnd	70
1		21	BattOut	BattOut	BattOut	BattOut	BattOut	BattOut	BattOut	BattOut	71
2 3		22	+5VSw	+ 12VSw	+5VSw	+ 12VSw	+5VSw	+ 12VSw	+5VSw	+ 12VSw	72
4	CharPwr	23	SpkrA	**	SpkrA	* *	SpkrA	* *	SpkrA	**	73
5 6	BattOut BattOut	24	SpkrB	+ 30v	SpkrB	+ 30v	SpkrB	+ 30v	SpkrB	+ 30v	74
f 7		25	+ 15VD	-15VD	+ 15VD	-15VD	+ 15VD	-15VD	+ 15VD	-15VD	75
9	+5VSw	26	*	ProcReset*	•	ProcReset*	٠	ProcReset*	•	ProcReset'	76
10 11		27	KbdRcv	KbdXmit	KbdRcv	KbdXmit	KbdRcv	KbdXmit	KbdRcv	KbdXmit	77
12	SpkrB	28	ModemR	ModemX	ModemR	ModemX	ModemR	ModemX	ModemR	ModemX	78
13 14	+30v (DC)← +5v	29_	MemComp	+5RelayOn'	MemComp	+5RelayOn'	MemComp	+5RelayOn'	MemComp	+5RelayOn'	79
15	6 KbdRcv	30_	Gnd	Gnd	Gnd	Gnd	Gnd	Gnd	Gnd	Gnd	80
16 17		31	MData00	+12RelayOn'	MData00	+12RelayOn*	MData00	+12RelayOn'	MData00	+12RelayOn'	81
18	GND	32_	MData01	Index*/Sec*	MData01	Index'/Sec'	MData01	Index'/Sec'	MData01	Index'/Sec'	82
19 20	,	33_	MData02	DS01'	MData02	DS01'	MData02	DS01'	MData02	DS01'	83
		34	MData03	DS02'	MData03	DS02'	MData03	DS02'	MData03	DS02'	84
		35_	MData04	DS03'	MData04	DS03,	MData04	D\$03'	MData04	DS03'	85
			MData05	MotorOn'	MData05	MotorOn'	MData05	MotorOn'	MData05	MotorOn'	86
			MData06	DirecSel'	MData06	DirecSel'	MData06	DirecSel'	MData06	DirecSel*	87
			MData07	Step'	MData07	Step'	MData07	Step'	MData07	Step'	88
s	A 450 Interface	39	MData08	WriteData'	MData08	WriteData'	MData08	WriteData'	MData08	WriteData'	89
	2 +SHBIBYUN	40	Gnd	Gnd	Gnd	Gnd	Gnd	Gnd	Gnd	Gnd	90
	6 ±12RelavOn'	41	MData09	WriteGate'	MData09	WriteGate'	MData09	WriteGate'	MData09	WriteGate'	91
	8 Index'/Sec'	42	MData10	Track00'	MData10	Track00'	MData10	Track00'	MData 10	Track00'	92
1	2 DSO2'	43	MData11	BusSync CorrOn'	MData11	BusSync CarrOn'	MData11	BusSync	MData11	BusSync	93 94
1	4 DS03'	44	MData12	CorrOn'	MData12	CorrOn'	MData12	CorrOn'	MData12	CorrOn	95
1	8 DirecSel!	45	MData13	BusClk	MData13	BusClk	MData13	BusClk Boset'	MData13	BusClk	
2	0 Step'	7	MData14	Reset'	MData14	Reset'	MData14	Reset'	MData 14	Reset'	96
2	A WriteGote'	47	MData15	WriteProt*	MData15	WriteProt'	MData15	WriteProt'	MData 15	WriteProt'	97
	6 Track00'	48	SideSel	ReadData'	SideSel	ReadData'	SideSel	ReadData'	SideSel	ReadData'	98 99
2 3	O ReadData'	49 50	+5v +5v	+5v +5v	+ 5v	+5v	+5v_ +5v	+ 5v	+5v +5v	+5v +5v	100
, <b>3</b>	2 SideSel				+ 5 v	+5v odem	1 + 5V   Disk & Di	+5v	I/Oprod		100
<b>~</b>		-	£	lattery	IVIC	A BIII	DISK & U	iopiay	17 0 0100	Spare I	Pins

**XEROX** Project File Designer Rev Date Page **Backpanel layout** SPG В 11/10/78 1 NoteTaker pntbp-1.sil Leung -Prototype

All odd no. pins GND

## View from etch side

( -	J5		J4		J3		J2		J1		
1	+ 12v + 12v		+ 12v + 12v		+ 12v + 12v		+12v +12v		+ 12v + 12v		51
2	+ 12v	+ 12 v	+ 12v	+ 12v	+ 12v	+ 12v	+ 12v	+ 12v	+ 12v	+ 12v	52
3	PageMode'	****	PageMode'								53
4	GoMem'	VSYNC'	GoMem'								54
5	-20V	-20 <b>V</b>	-20V	-20V	-20 <b>V</b>	-20V	-20V	-20V	-20V	-20V	55
6	BusLock'	Videα	BusLock'	CAS		CAS		CAS		CAS	56
7	BusClkDly'	HSynic	BusClkDly'	Wkrite	BusClkDly'	Write	BusClkDly'	Write	BusClkDly'	Write	57
8	ProcBoot'	ParErr	ProcBoot'	ParErr	Data00	Data00	Data00	Data20	Data20	Data20	58
9	ProcInt'	DataReady	Procint'	DataReady	Data01	Data01	Data01	Data21	Data21	Data21	59
10	Gnd	Gnd	Gnd	Gnd	Gnd	Gnd	Gnd	Gnd	Gnd	Gnd	60
11	BusReq0'	BusReq4'	BusReq0'	BusReq4'	Data02	Data02	Data02	Data22	Data22	Data22	61
12	BusReq1'	BusReq5'	BusReq1'	BusReq5'	Data03	Data03	Data03	Data23	Data23	Data23	62
13	BusReq2'	BusReq6'	BusReq2	BusReq6*	Data04	Data04	Data04	Data24	Data24	Data24	63
14	BusReq3'	BusReq7'	BusReg3'	BusReq7'	Data05	Data05	Data05	Data25	Data25	Data25	64
15	Bootsw+	TABXO	Bootsw+	TABXO	Data06	Data06	Data06	Data26	Data26	Data26	65
16	Bootsw-	TABYO	Bootsw-	TABYO	Data07	Data07	Data07	Data27	Data27	Data27	66
17	CharCtr	TABX1	CharCtr	TABX1	Data08	Data08	Data08	Data28	Data28	Data28	67
18	CharPwr	TABY1	CharPwr	TABY1	Data09	Data09	Data09	Data29	Data29	Data29	68
19	96Khz	***	96Khz	***	Data10	Data10	Data10	Data30	Data30	Data30	69
20	Gnd	Gnd	Gnd	Gnd	Gnd	Gnd	Gnd	Gnd	Gnd	Gnd	70
21	BattOut	BattOut	BattOut	BattOut	Data 11	Data 11	Data 11	Data31	Data31	Data31	71
2.2	+ 5VSw	+ 12VSw	+5VSw	+ 12VSw	Data12	Data12	Data12	Data32	Data32	Data32	72
23	SpkrA	**	SpkrA	**	Data13	Data13	Data13	Data33	Data33	Data33	73
24	SpkrB	+ 30v	SpkrB	+ 30v	Data14	Data 14	Data 14	Data34	Data34	Data34	74
^5_	+ 15VD	-15VD	+ 15VD	-15VD	Data15	Data 15	Data 15	Data35	Data35	Data35	75
<u> 76</u>	•	ProcReset'	*	ProcReset*	Data16	Data 16	Data 16	Data36	Data36	Data36	76
27	KbdRcv	KbdXmit	KbdRcv	KbdXmit	Data17	Data 17	Data 17	Data37	Data37	Data37	77
28	ModemR	ModemX	ModemR	ModemX	Data18	Data 18	Data 18	Data38	Data38	Data38	78
29	MemComp	+5RelayOn'	MemComp		Data 19	Data 19	Data 19	Data39	Data39	Data39	79
30	Gnd	Gnd	Gnd	Gnd	Gnd	Gnd	Gnd	Gnd	Gnd	Gnd	80
31	MData00	+ 1 2RelayOn'	MData00	MAO'	MData00	MAO'	MData00	MAO'	MData00	MAO'	81
32	MData01	Index'/Sec'	MData01	MA1	MData01	MA1	MData01	MA1'	MData01	MA1'	82
33	MData02	DS01'	MData02	MA2'	MData02	MA2	MData02	MA2'	MData02	MA2	83
34	MData03	DS02'	MData03	MA3'	MData03	MA3.	MData03	MA3.	MData03	MA3'	84
35	MData04	DS03'	MData04	MA4'	MData04	MA4'	MData04	MA4'	MData04	MA4'	85
36	MData05	MotorOn'	MData05	MA5'	MData05	MA5'	MData05	MA5'	MData05	MA5'	86
37	MData06	DirecSel'	MData06	MA6'	MData06	MA6'	MData06	MA6'	MData06	MA6'	87
38	MData07	Step*	MData07	MA7'	MData07	MA7	MData07	MA7'	MData07	MA7'	88
39		WriteData'	MData08	MAE'	MData08	MAE'	MData08	MAE'	MData08	MAE'	89
40		Gnd	Gnd	Gnd	Gnd	Gnd	Gnd	Gnd	Gnd	Gnd	90
41	MData09	WriteGate'	MData09	RASO	MData09	RASO_	MData09	RASO	MData09	RASO	91
42	MData10	Track00'	MData 10	RAS1	MData10	RAS1	MData10	RAS1	MData10	RAS1	92
43	MData11	BusSync	MData11	BusSync	MData11	BusSync	MData11	BusSync CorrOn'	MData11	BusSync	93
44	MData12	CorrOn'	MData12	CorrOn'	MData12	CorrOn'	MData12	CorrOn'	MData12	CorrOn'	94
45	MData13	BusClk	MData13	BusClk	MData13	BusClk	MData13	BusClk	MData13	BusClk	95
46	MData14	Reset'	MData14	Reset'	MData14	Reset*	MData14	Reset'	MData14	Reset'	96 97
47	MData15	WriteProt'	MData15	RAS2	MData15	RAS2	MData15	RAS2	MData15	RAS2	
48	SideSel	ReadData'	. 57	RAS3	. 5	RAS3	. 5	RAS3	. 5 4	RAS3	98
49	+5v +5v	+ 5v	+5v	+5٧	+5v	+5v	+ 5v	+5v	+5v	+ 5 v	99 100
<u>50</u>	7 J V	+ 5v	+5v	+ 5v	+ 5 v	+ 5v	+5v	+5v	+5v	+ 5 <b>v</b>	, 100

 ${\bf Emulator\, Proc.}$ 

Mem. Control

Mem. Storage-1

Mem. Data

Mem. Storage-2

XEROX	Project	Backpanel Layout	File	Designer	Rev	Date	Page
SPG	NoteTaker	-Prototype	PNTBP-2.SIL	Leung	В	9/22/78	2